REMARKS

Entry of the foregoing amendment and following remarks are respectfully requested. Upon entry of this amendment, claims 1-21 and 23-47 will remain pending in this application.

Applicants thank the Examiner for the telephonic interview of October 9, 2001, at which interview the rejections under 35 USC 101 and 103 were discussed.

Claims 21-30 stand rejected under 35 USC 101 as being directed to non-statutory subject matter. Applicant respectfully traverses this rejection.

The inventions of claims 21 -30, as most broadly defined by independent claim 21, requires, among other elements, a root containing at least one library, and all of the other elements within the recited computer readable medium are related to this root. The claimed structure allows, within the same structure, elements that are needed to represent the digital circuit at various stages of the design process. As set forth previously in claim 22, which has been cancelled and placed into claim 21, these elements are recited as being used to create a data model, which created data model includes both logical synthesis information and physical placement information. Thus, a relationship exists within the recited structure, since together it provides for a novel circuit description that describes the digital circuit. Accordingly, there is a functional interrelationship with respect to the various data elements, since together they are used to obtain the representation of the digital circuit. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-6 and 14-20 stand rejected under 35 USC 102(b) as being anticipated by Rostoker US Patent No. 5,541,849. Applicants respectfully traverse the Examiner's grounds of rejection.

Independent claim 1 requires processing a description of the circuit in a computer system to generate electrical signals representative of a data model including information on logical parameters of the circuit and information on physical parameters of the circuit. As thus defined, it is clear that the same data model must include both logical and physical parameters of the circuit. The '849 patent does not provide such a data model. While the Examiner points to the VHDL compiler and simulator and design partitioner (blocks 904 and 908). As is apparent from the text provided that relates to blocks 904 and 908 of Fig. 9, these blocks are shown as a "conceptual level" that shows a "generalized methodology" of the invention of the '849 patent (see column 16, lines 40-45). This does not show, however, a data model that provides information on including logical and physical parameters of the circuit. As is conventional, there is a separate model for each in the '849 patent --- the VHDL for the logical parameters, and the separate netlist for the physical parameters. That these are separated is apparent from the description at column 10, lines 62-64 where is indicated that "[S]tep 8 is Synthesis.

Given the module description (step 7) and a target technology library, the design is mapped into the target technology." And as described, there is no data model that contains information from both the module description and the target technology. Thus, the '849 patent does not contain "a data model" that contains parameters that include both logical and physical parameters. Accordingly, it is respectfully submitted that claim 21, and the claims dependent thereon, contain allowable subject matter.

Claims 21-30 stand rejected under 35 USC 102(b) as being anticipated by Mahmood US Patent No. 5,762,902. Applicants respectfully traverse the Examiner's grounds of rejection.

As noted above, independent claim 21, requires, among other elements, a root containing at least one library, and all of the other elements within the recited computer readable medium are related to this root. The claimed structure allows, within the same structure, elements that are needed to represent the digital circuit at various stages of the design process. Further, the information within each model include both logical synthesis information and physical placement information. The '902 patent, like the '849 does not include a data model that includes both logical synthesis information and physical placement information. Like the '902 patent, these are separated into different models. Accordingly, it is respectfully submitted that claim 21, and the claims dependent thereon, contain allowable subject matter.

Applicants also bring to the Examiner's attention new claims 31-47 that have been added to the application, and which are believed to contain patentably distinct subject matter.

In view of the above amendments and remarks, Applicants submit that the above-referenced application is in a condition for allowance, and such a Notice is respectfully requested.

Respectfully submitted,
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I certify that this paper is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on October 9, 2001. [redacted]

Maria English

APPENDIX

The following claim illustrates the changes made using brackets [] for deleted text and underline for new text added to the claim:

21. (amended) A computer-readable medium storing a data structure for representing digital circuits, wherein:

the data structure includes a root containing at least one library;

each library contains at least one entity;

each entity contains at least one model and at least one port;

each model contains at least one cell, at least one net and at least one model pin; [and]

each cell contains at least one cell pin; and

wherein the data structure is used to create a data model representing a digital circuit, which data model includes the at least one cell pin, the at least one cell, the at least one net, the at least one model pin and the at least one port, which are obtained by selecting the at least one library within the root, the at least one entity, and the at least one model, and wherein the data model thus created includes both logical synthesis information and physical placement information.